Ania K. Mitros, Ph.D.

275 Chiquita Ave
Mountain View, CA 94041

(206) 619-1500
ania.mitros@gmail.com

Overview

Electrical engineer experienced in high voltage battery monitoring systems (BMS), including safety and the full ASIC development cycle. At Continental, I performed various architecture, system, and safety analyses. At Tesla, I was responsible for the ASICs at the core of a more accurate, more robust, and less costly BMS than the previous generation. At Maxim, I designed the analog circuits inside BMS chips, and did some R&D projects. I prefer roles with both breadth and depth, including system-level evaluation, collaboration across engineering groups, and technical deep dives into data and design.

Work and Research experience

- **Continental Automotive** (May 2018–present) Though hired into the innovation organization, I work closely with the product design groups. I do technical analyses to refine the development roadmap, assess which chips fit which projects, and help re-evalute the safety case under ISO26262.
- **Tesla Battery Engineering:** (Oct 2014–Apr 2018) I was responsible for the ASICs that measure voltages and temperatures in the Model 3 high voltage battery. My role included the full product cycle: defining requirements, evaluating cost trade-offs, vendor selection, analysis of ASIC test data, fault tree analysis, diagnostics definition, collaboration with firmware, design reviews of the PCBAs, legal contract development, Python and MySql queries to analyze vehicle field data and manufacturing test data, setting manufacturing test limits, reliability evaluation, introduction to mass production, and general shepherding. I enjoyed the breadth and collaboration of this role combined with its very technical underpinning.
- **Maxim, Analog Power Management IC Design:** (Sept 2006–July 2013) Analog design for battery management ICs, both consumer (2-4 cell) and automotive (12 cell: MAX11068, MAX17823). My circuits included: sub-1.7V bandgap, linear regulator, comparator, charge pumps, redesign of an EEPROM block from another design group while the original block was in qualification and continual changes, capacitively-coupled I2C interface for the MAX11068, supervision of layout, bench testing of silicon. R&D tasks included design and layout of experimental ESD structures, debugging of latchup and snap-back in a high voltage process, defining an automated latchup error deck within the standard DRC flow, and package stress experiments to improve reference accuracy. Additionally, I started and lead a lunch seminar series which grew to host around 100 people. Founding member of Maxim's Green Team. Continually initiated changes by the EDA group to our internal design tools.
- **Caltech PhD:** I designed and tested four VLSI chips with analog in-pixel image processing. Two chips were at Caltech under Prof Christof Koch, and two at the Univ. of Washington co-advised by Profs Chris Diorio and Christof Koch.
  Vibrating Retina: I developed an on-chip imager for feature detection at sub-pixel resolution by taking advantage of mechanical vibrations. Tasks included design, transistor layout in Cadence, and testing of an asynchronous digital VLSI block for communication;

testing of chip; AutoCAD design of mechanical system to induce the vibrations; and system simulations in Matlab.
Feature Detector: I designed and tested a CMOS imager chip with in-pixel analog preprocessing and floating gates (EEPROM) programmed to analog values to remove mismatch. Floating-gates reduced mismatch in photoreceptor, Gilbert multiplier, and analog differencing circuit. I used Matlab for system simulation, Cadence for transistor-level circuit simulation and layout, and microcontroller and Matlab for testing.

- ◇ **Neurochip:** (Caltech, winter term 1999) Implanted neurons onto silicon chip for extracellular stimulation and recording in lab of Prof. Jerome Pine.
- ◇ **VLSI CPG:** (Los Alamos National Laboratory, summer 1997) Implemented central pattern generator (CPG) using discrete analog components. Learned MAGIC to design and lay out a successful CPG chip.
- ◇ **C++ Programming** (Texas Instruments, summer 1996) Wrote COFEY (Correlation Of Final Eval and Yield), an object-oriented application to extract data from two servers, perform statistical analyses, graph the data, and save in a standard format. COFEY was in use for years.

Education

- ◇ **California Institute of Technology Ph.D.** in Computation and Neural Systems; advised by Professors Christof Koch (Caltech) and Chris Diorio (Univ. of Washington). Defended Feb. 15, 2006.
- ◇ **Rice University B.A.** Computer Science, 1998.
- ◇ **Westlake High School.** 1994. Class rank: 9/406
- ◇ **Online** Sept-Dec 2013
  - · "Introduction to Power Electronics" by Prof Erickson, UC Boulder, Coursera
  - · "Solar Cells, Fuel Cells and Batteries" by Prof Clemens, Stanford OpenEdX
  - · "Inspiring Leadership through Emotional Intelligence" by Prof Boyatzis, Case Western, Coursera

Published

- ◇ **L**andolt O., Mitros A. "Visual sensor with resolution enhancement by mechanical vibrations" *Autonomous Robots* (Nov 2001), 11 (3): 233-239.
- ◇ **L**andolt O., Mitros A., Koch C. "Visual Sensor with Resolution Enhancement by Mechanical Vibrations" *Proceedings 2001 Conference on Advanced Research in VLSI*, 249-264.

Teaching

- ◇ **Workshop Tutorial** (July 2003) Taught floating gate transistor tutorial at 2003 Telluride Neuromorphic Engineering Workshop.
- ◇ **Community Outreach** (March 2005-Aug 2006) Designed and taught hands-on lesson on electronics to kids.
- ◇ **Teaching Assistant**
  - · CNS 185 (1999): Collective Computation (neural models and neural networks)
  - · CNS 187 (2000): Neural Computation (successor to CNS 185)