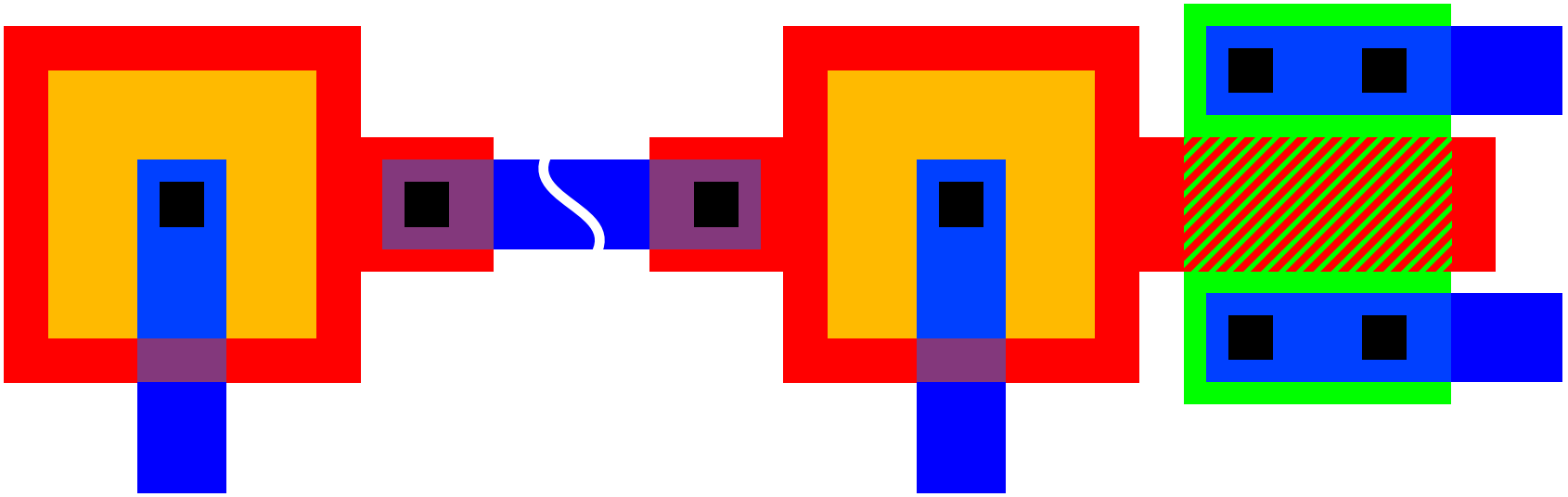
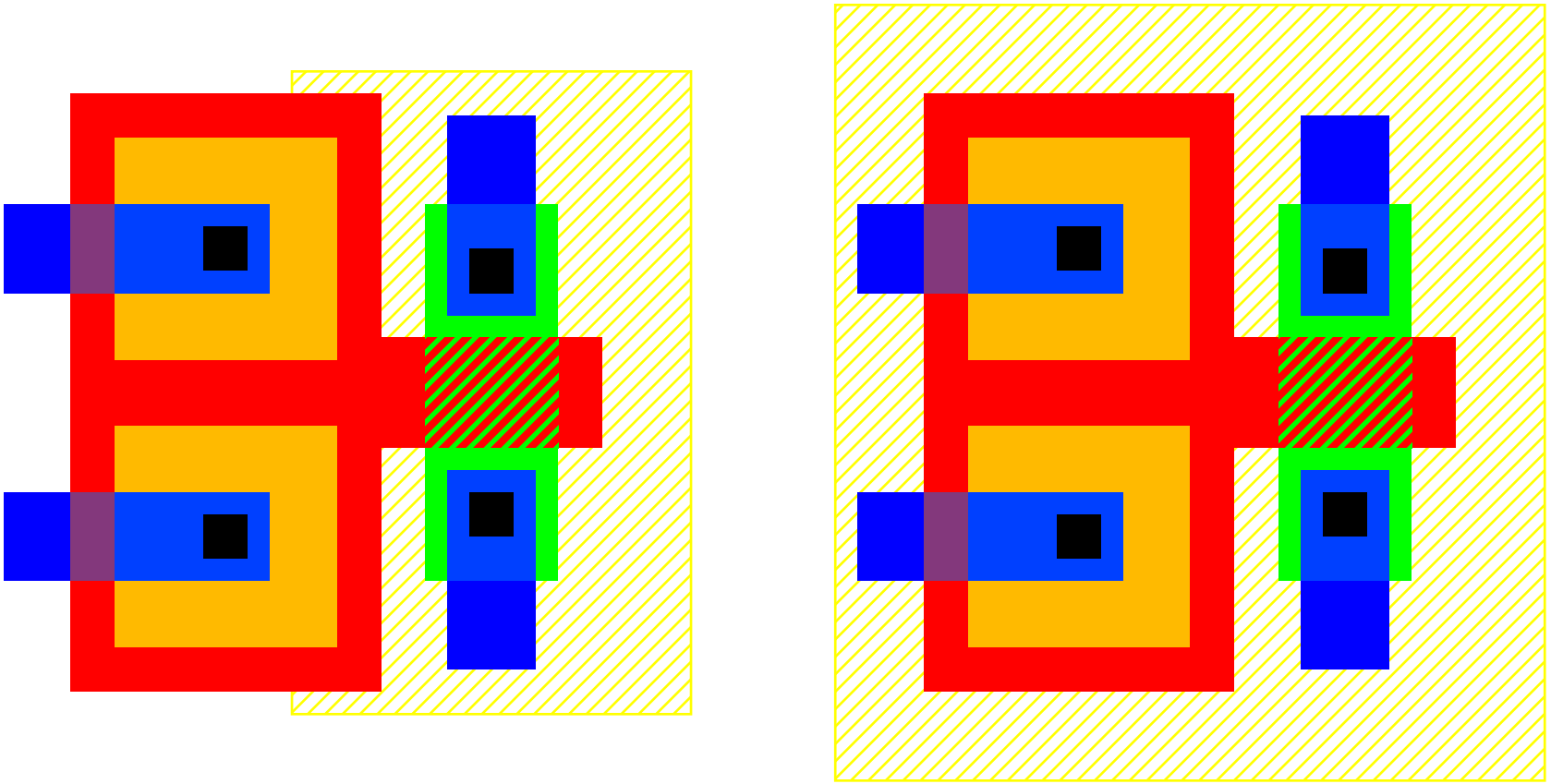
How to Make Leaky Floating Gates...



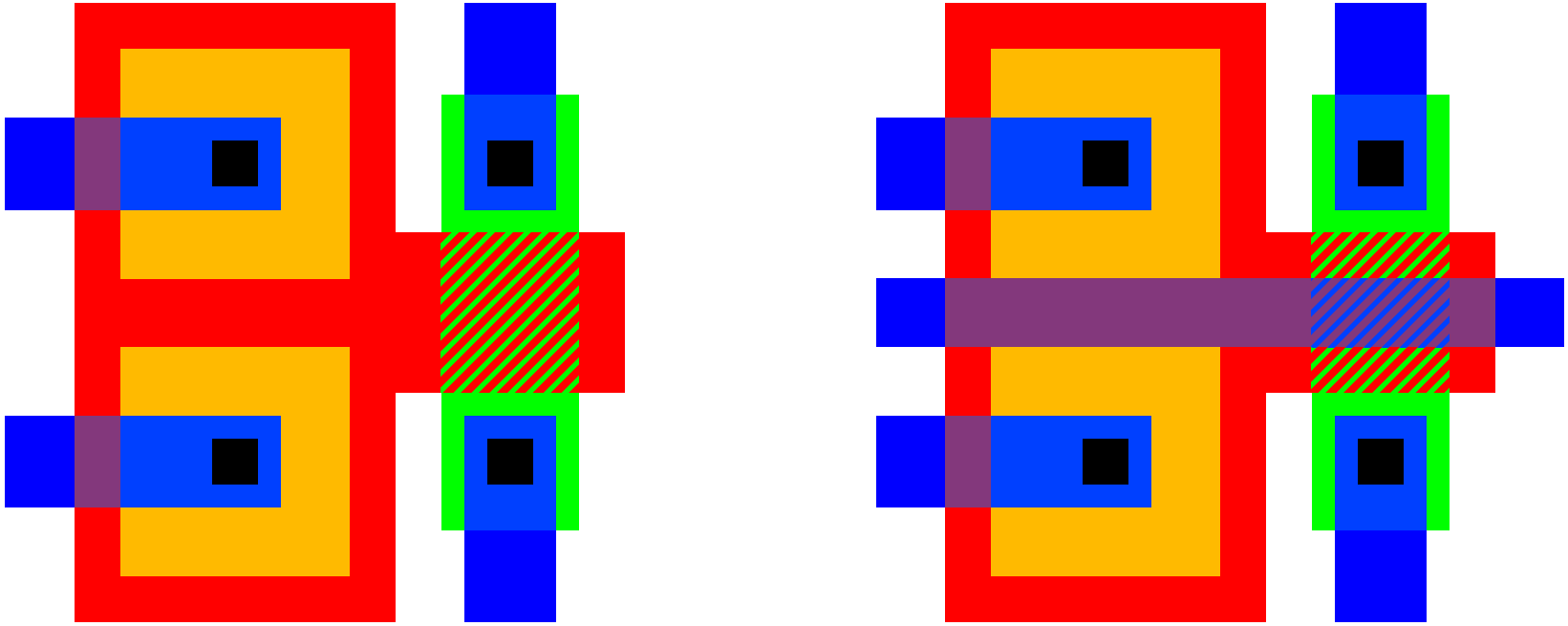
- Keep your floating gates on poly1.
- If you make a contact to metal, your gate will probably leak, because the oxide surrounding the metal layers are typically deposited rather than thermally grown.

Beware of Capacitive Coupling from Below...



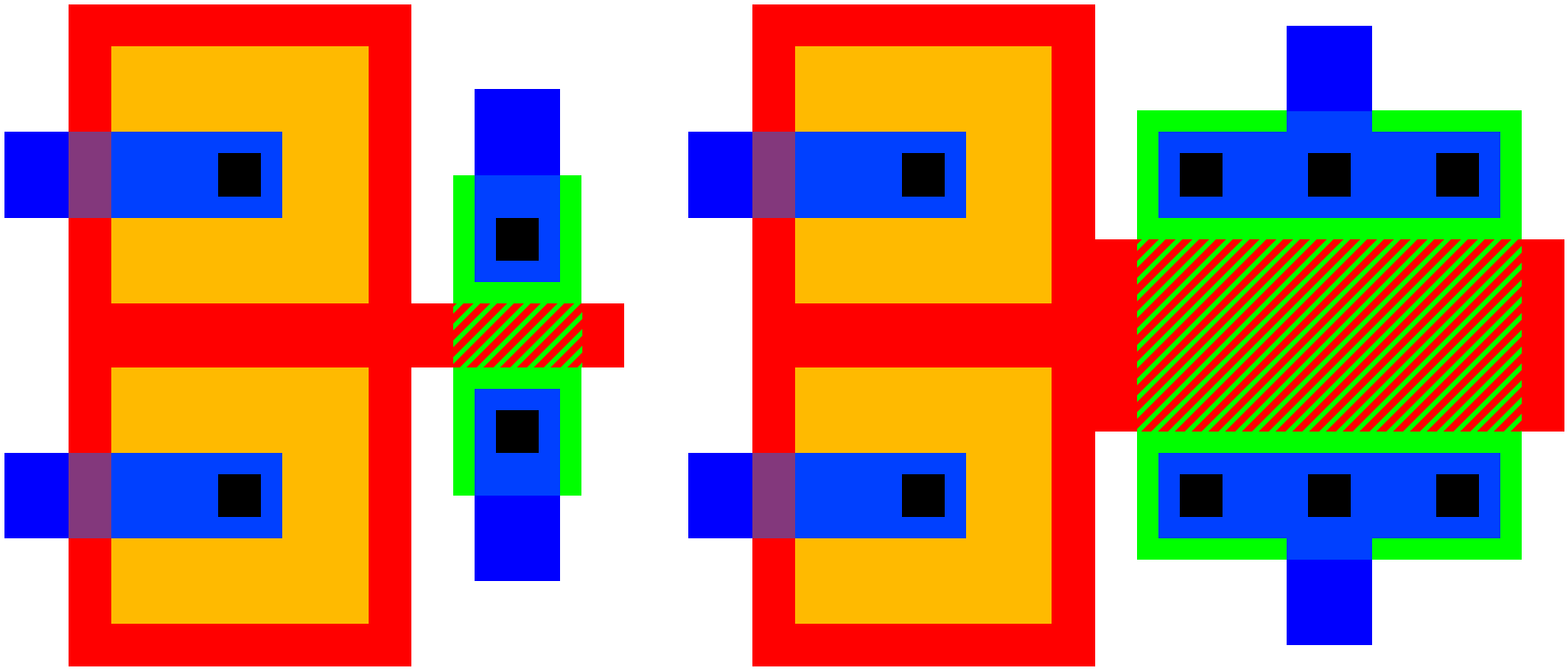
- If possible, don't allow a floating gate to cross a well boundary. For a *p*FGMOS, keep it entirely over the well. For an *n*FGMOS, keep it entirely over the substrate.
- If you split the area evenly between the substrate and the well, your floating-gate voltage will have a dependence on V_{DD} that you didn't expect...

Beware of Capacitive Coupling from Above...



- Be careful about routing metal lines over top of your floating gates. The voltages on such lines couple into the floating gate just like the control-gate voltages.
- Moreover, if you are trying to carefuly match C_T for two FGMOS transistors, then you have to count the stray capacitance between these lines and the floating-gate too...

Which FGMOS Transistor Has a Higher Output Resistance?



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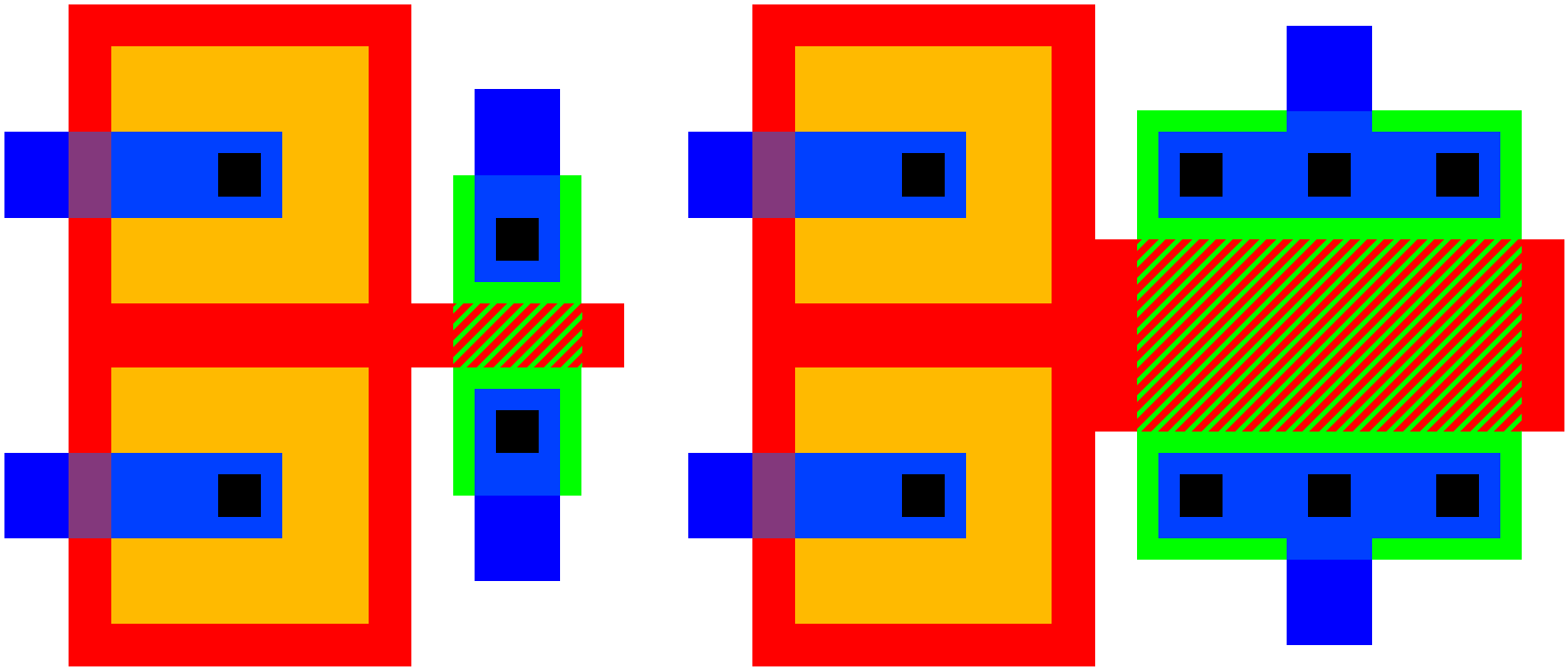
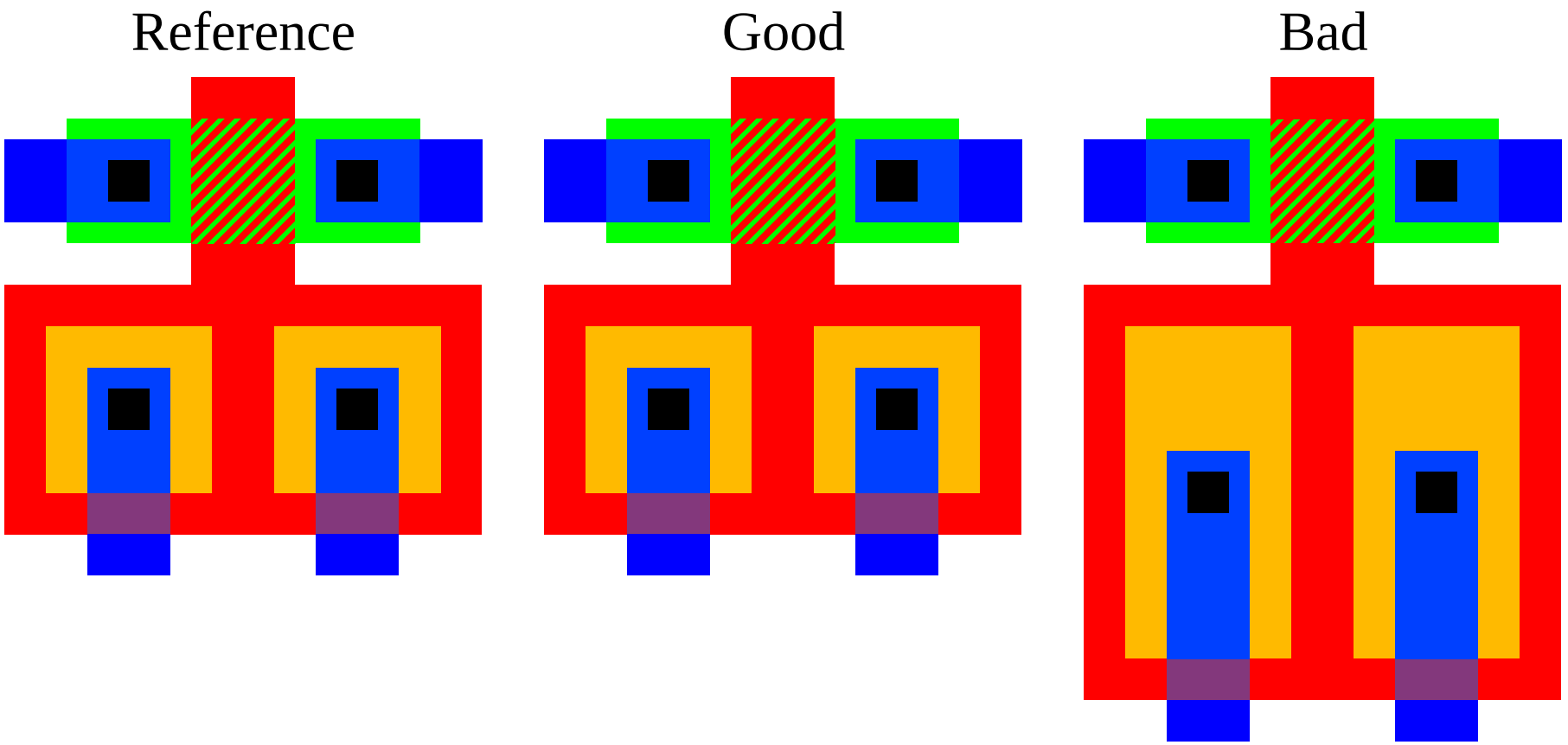


- The transistor on the *left*...
- For a FGMOS transistor, the Early effect (i.e., channel-length modulation) is always negligible compared to the effect of V_D coupling through C_{gd} to the floating gate. Increasing L does *not* increase r_o.
- $C_{gd} \propto W$, so making the transistor wider *decreases* r_o.

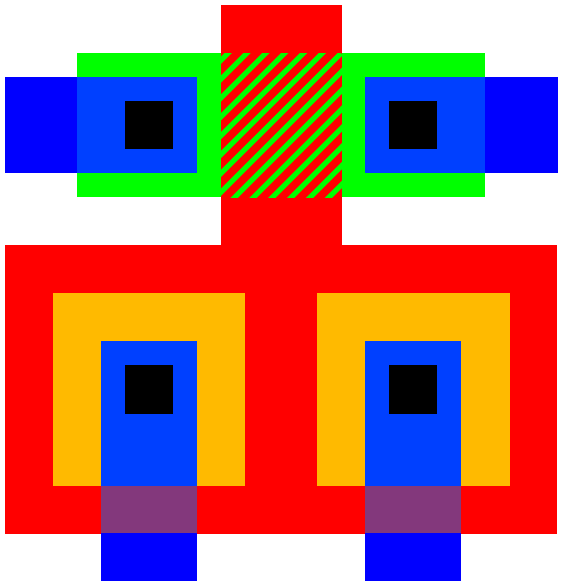
Matching: Same Size & Shape



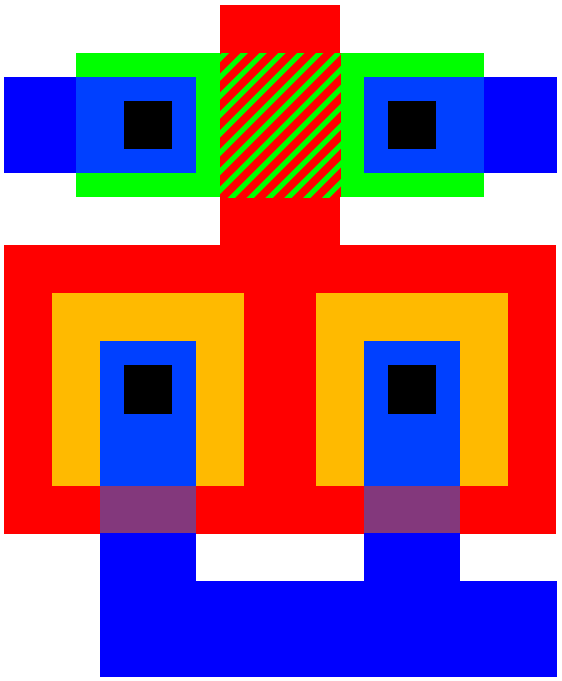
- To obtain matched capacitive-divider ratios in different FGMOS transistors, use floating gates with identical geometries.
- Don't forget that C_T includes parasitics that you won't be able to predict properly at design time.

Matching: Parallel Unit-Sized Control Gates

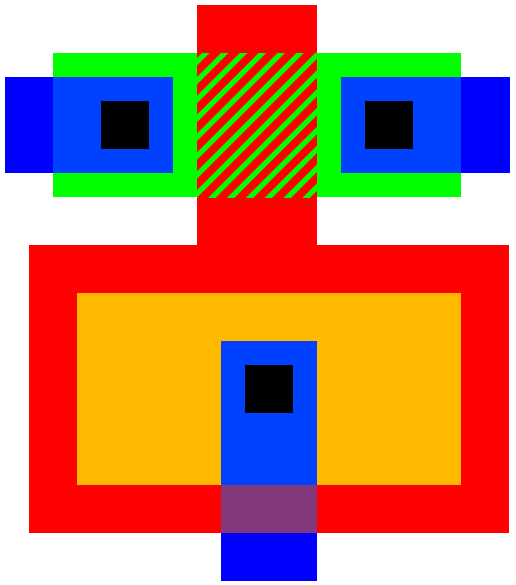
Refernce



Good

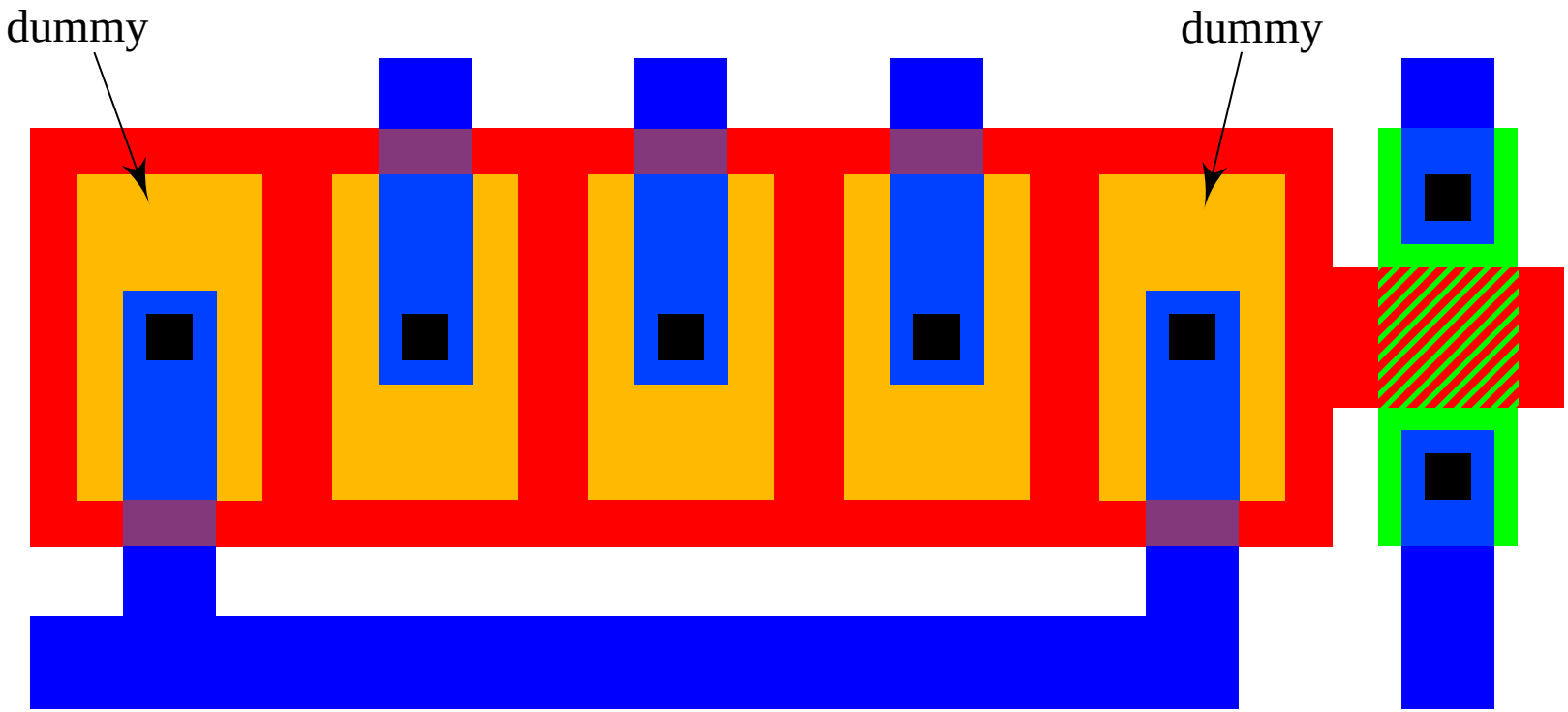


Bad



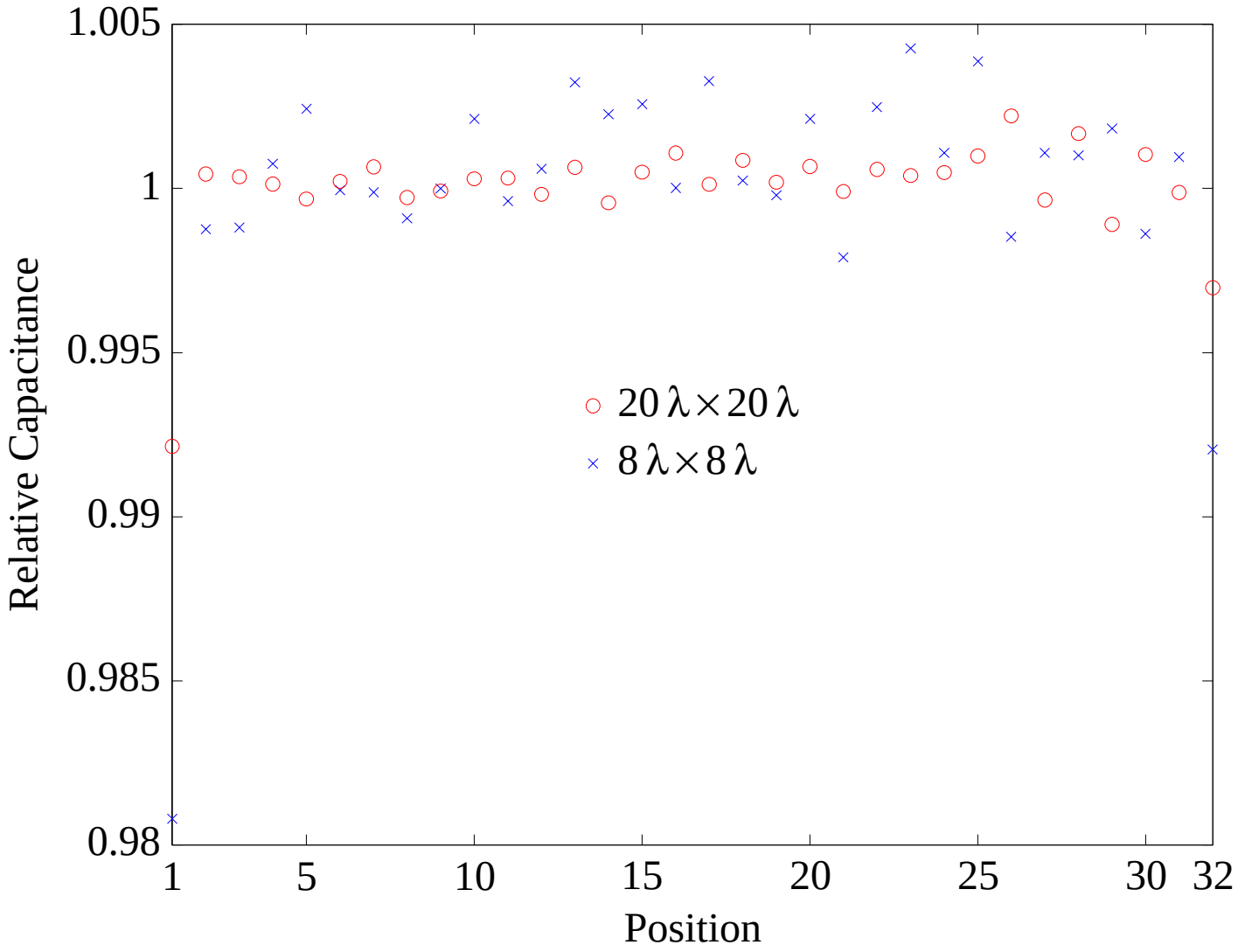
- To obtain accurate control-gate capacitor ratios (e.g., 2:1), connect unit-sized control gates in parallel rather than making composite control gates with the correct area ratios.
- If you are trying to carefuly match C_T, don't connect the unit-sized control gates on top of the floating gate.

Matching: Same Surround



- To improve control-gate matching, use “dummy” control gates at each end to make each “real” control gate have an identical surround.
- Systematic edge effects are ubiquitous, but the underlying mechanisms are not always clear (e.g., fringing fields, non-uniform etching rates).

Relative Capacitance vs Position (1.2–μm Process)



Relative Capacitance vs Position (.35–μm Process)