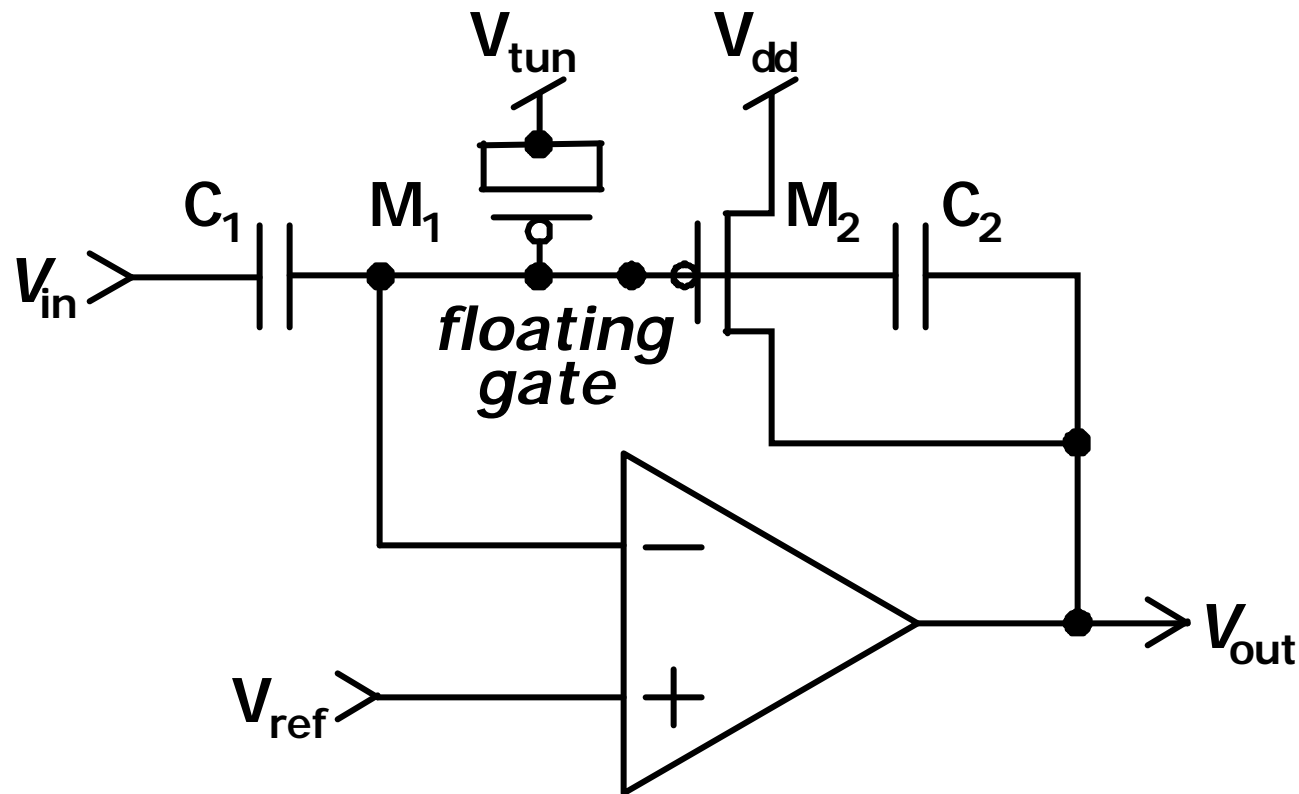


Some applications with FGs

- Autonulling amplifier (Hasler et al 2001, Rahimi et al 2002)
- Learning with probabilities (Hsu)
- Mismatch reduction (Mitros)
- Automaximizing bump circuit, and learning the means of a mixture of Gaussians (Hsu)

Autonulling Amplifier

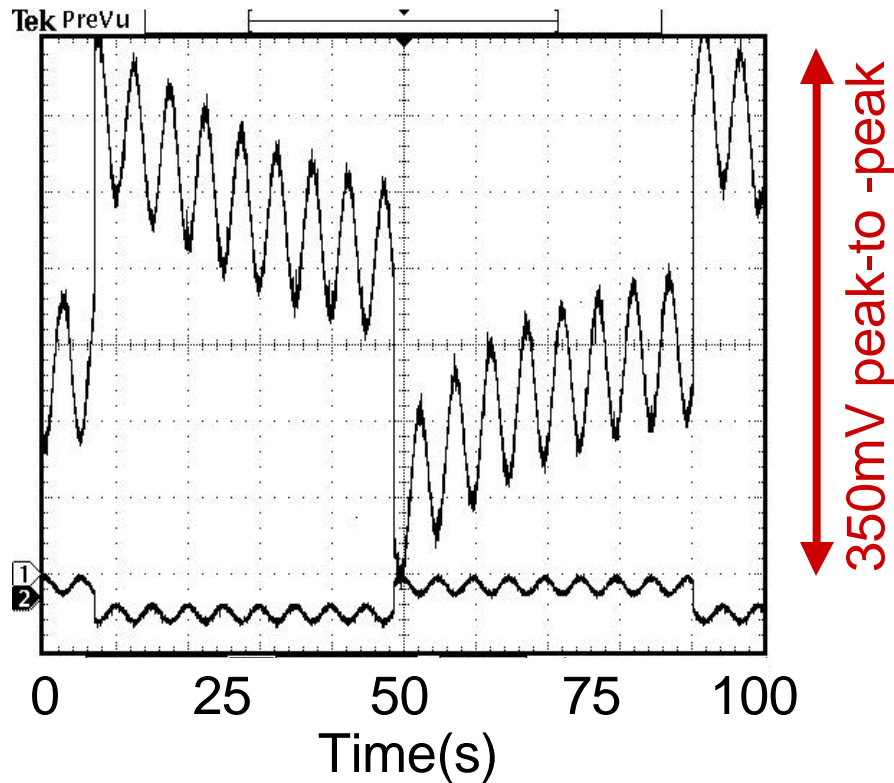


- AC coupled with a $\sim 0.1\text{Hz}$ corner
 - Tunneling/IHEI sets DC output voltage
 - Capacitive ratio $-C_1/C_2$ sets amplifier gain

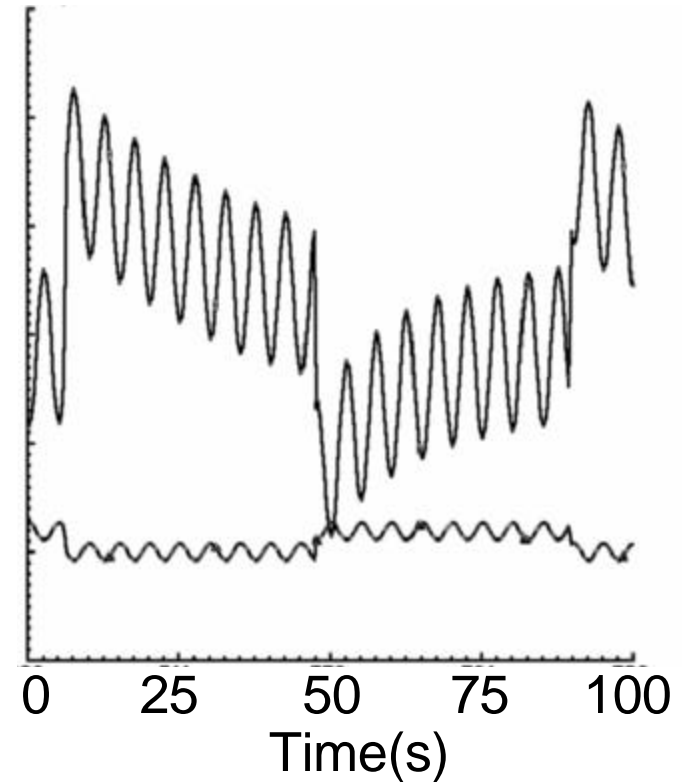
see Rahimi et al, 2002

Amp Circuit Data and Simulation

Measured circuit response



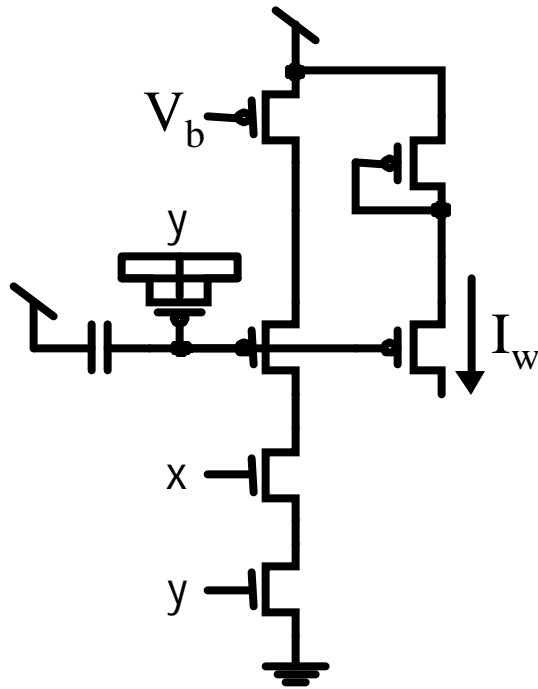
SPICE simulation



- Input: 0.2 Hz, 15mV sinewave superimposed on a 0.012 Hz, 19mV square-wave

see Rahimi et al, 2002

Learning a Conditional Probability



$$P(V_{tun}) = P(y)$$

$$P(V_{inj}) = P(x, y)$$

$$I_{out} = I_0 e^{-V_{FG}}$$

$$I_{inj} = \mathbf{I} (e^{-V_{FG}})^f P(X, Y) = \mathbf{I} I_0^f I_{out}^{-f} P(X, Y)$$

$$I_{tun} = \mathbf{h} (e^{V_{FG}})^n P(Y) = \mathbf{h} I_0^{-n} I_{out}^n P(Y)$$

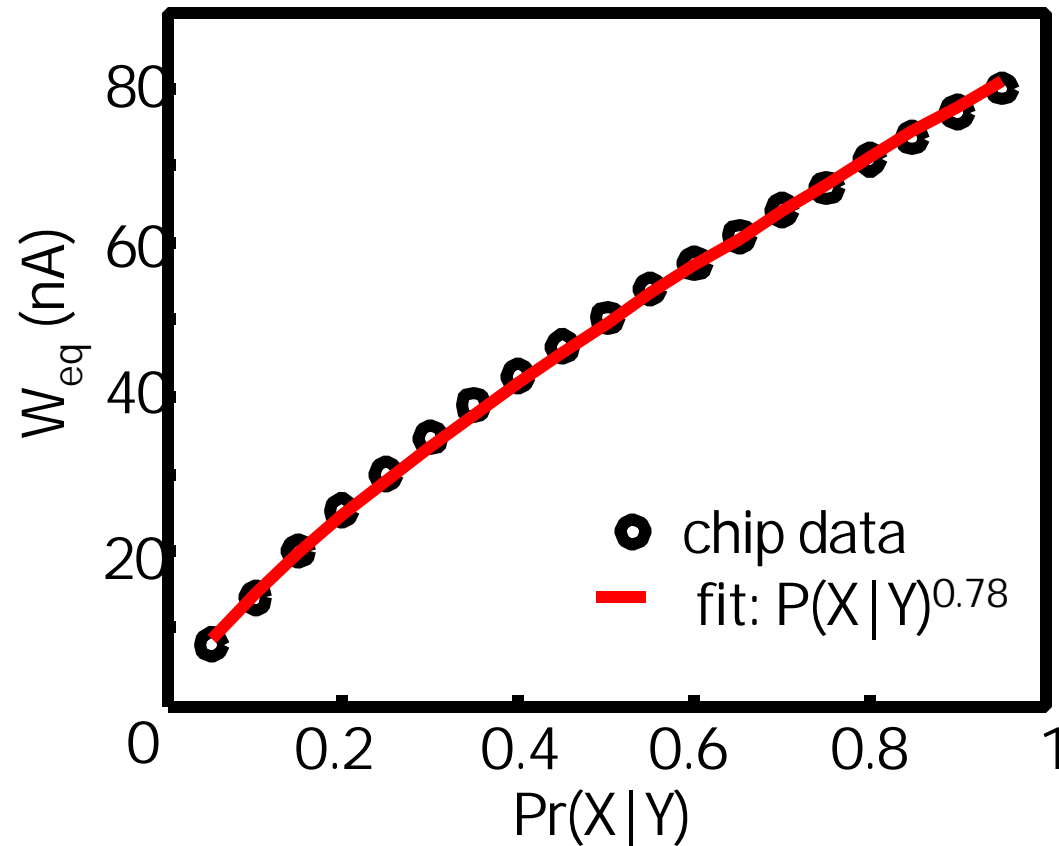
$$I_{inj} = I_{tun} \rightarrow I_{out} = I_0 \left(\frac{\mathbf{I} P(X, Y)}{\mathbf{h} P(Y)} \right)^{\frac{1}{f+n}}$$

$$I_w \propto \left(\frac{P(V_{inj})}{P(V_{tun})} \right)^s \propto \left(\frac{P(x, y)}{P(y)} \right)^s \propto (P(x | y))^s$$

"Learning Spike-Based Correlations and Conditional Probabilities in Silicon"
 Aaron Shon, Dave Hsu, and Chris Diorio. *In Proc. NIPS 2001*

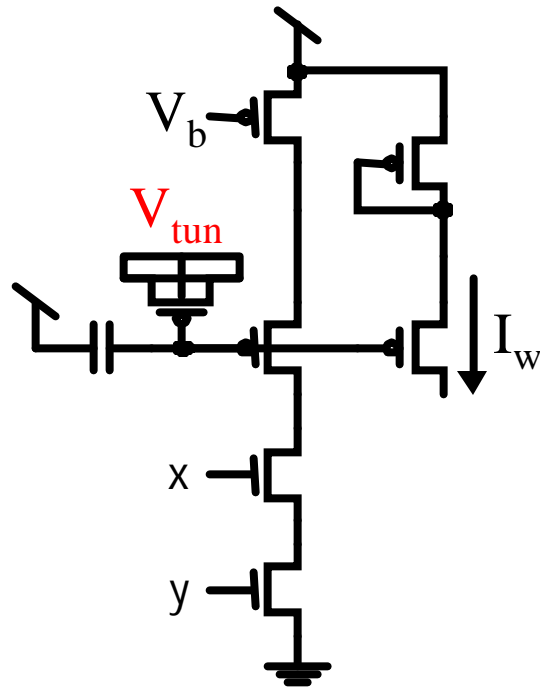
Circuit data for $P(X|Y)$

Equilibrium weight versus input statistics



"Learning Spike-Based Correlations and Conditional Probabilities in Silicon"
Aaron Shon, Dave Hsu, and Chris Diorio. *In Proc. NIPS 2001*

Learning Correlations



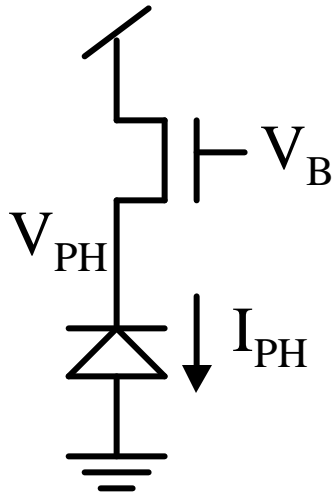
Let V_{tun} be constant (like leakage current).
The circuit learns the correlation between
X and Y.

$$I_w = (P(V_{inj}))^s = (P(x, y))^s$$

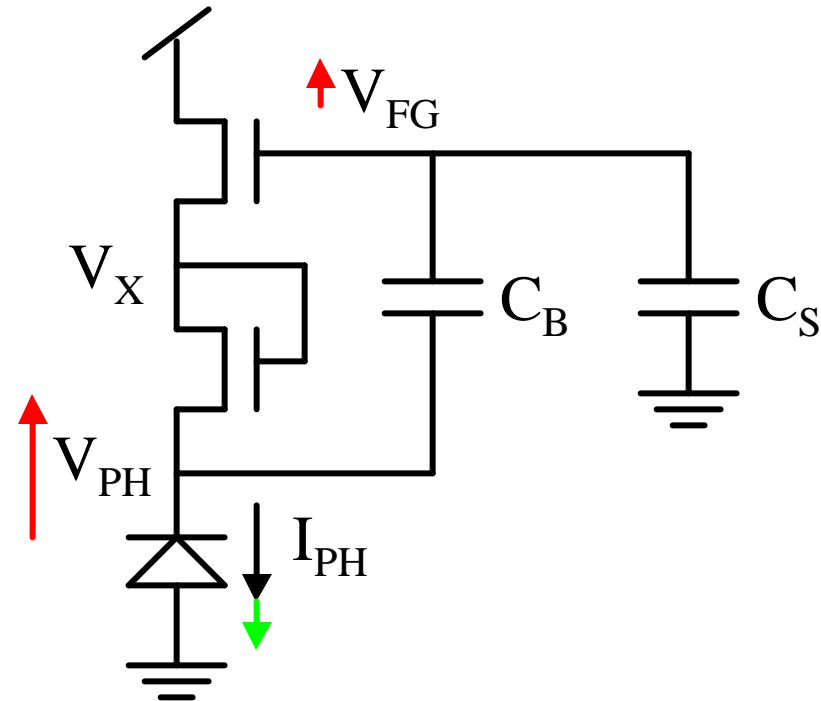
Mismatch reduction

- Standard techniques for improving mismatch require a lot of die area:
 - dummy transistors
 - common-centroid layout
 - large transistors (or multiple copies)
- Charge on floating gate is equivalent to changing V_{TH} . Floating gates allow use of minimum size transistors and programming away of most of the mismatch as long as mismatch is mainly due to V_{TH} mismatch rather than gain mismatch (true for circuits I've dealt with).

Logarithmic photoreceptors

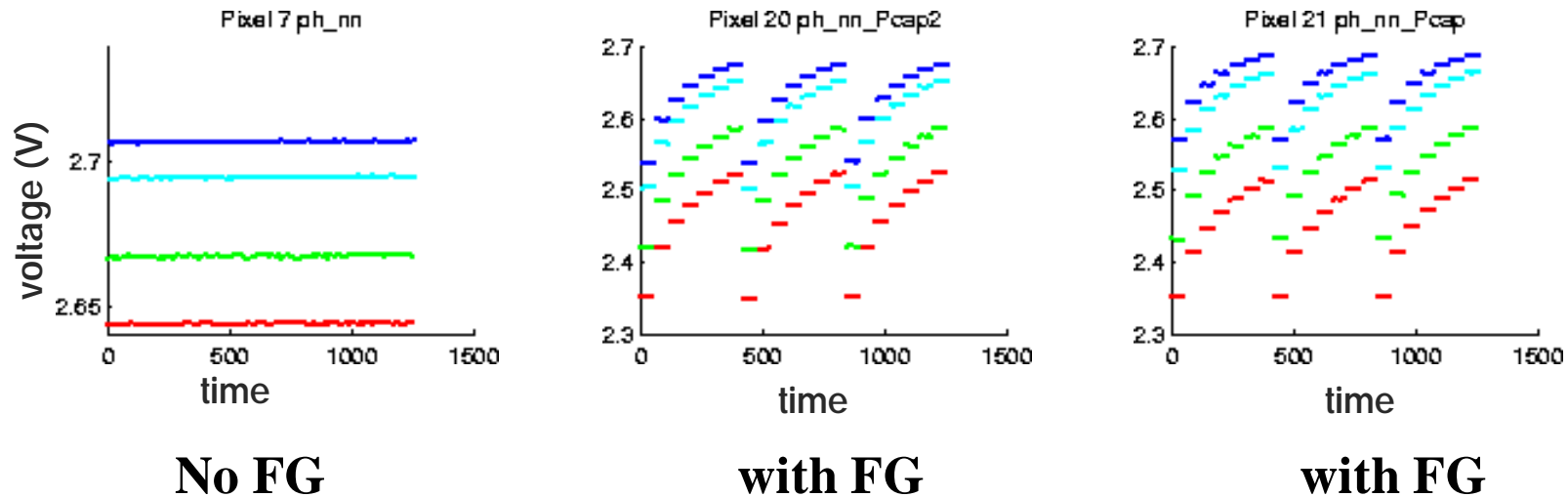


$$V_{PH} = -\log\left(\frac{I_{PH}}{I_0}\right)$$



$$V_{PH} = -2\left(\frac{C_S + C_B}{C_S}\right) \log\left(\frac{I_{PH}}{I_0}\right)$$

Photoreceptor: shifting DC level



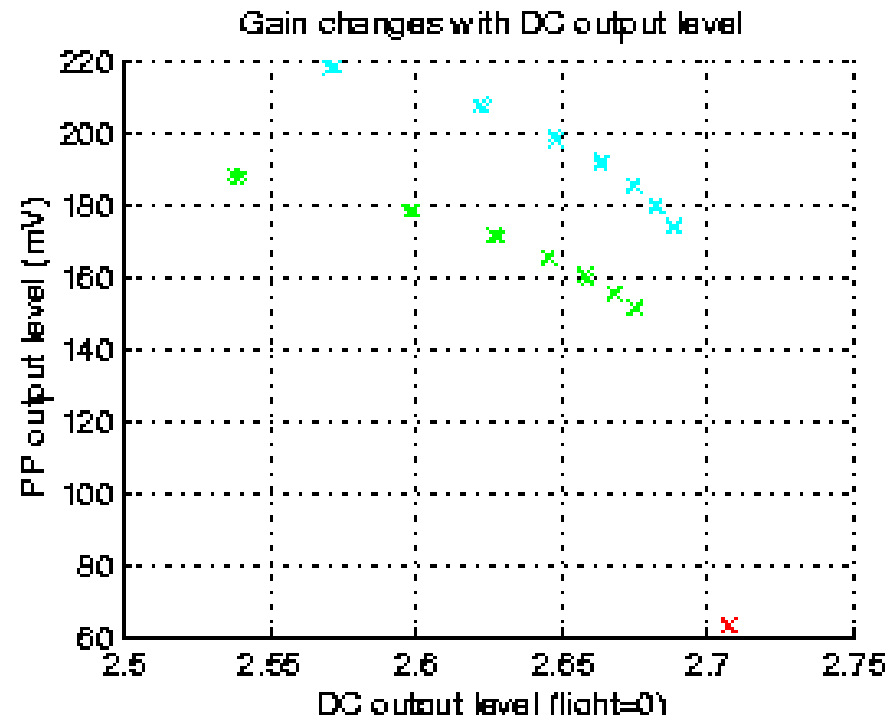
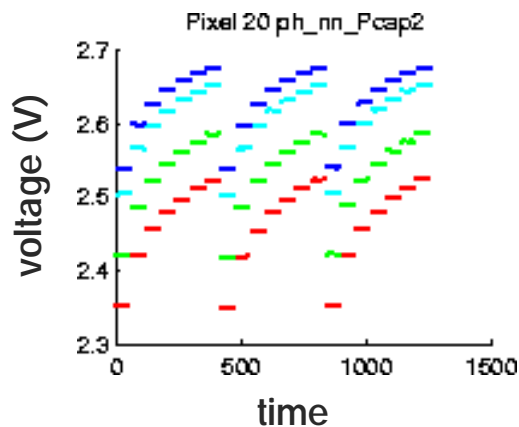
The data collection procedure was as follows: 6 tunneling pulses, 1 injection pulse, 6 tun, 1 inj, 6 tun. Several data points were collected between each programming pulse. The plots show data as a function of time. Each upward vertical jump in the data corresponds to the result of a tunneling pulse. Each downward jump corresponds to injection. Colors represent intensity of LCD monitor: Dark blue=0 (darkest), Cyan=21, Green=42, Red=63 (brightest).

Photoreceptor: effect on AC gain

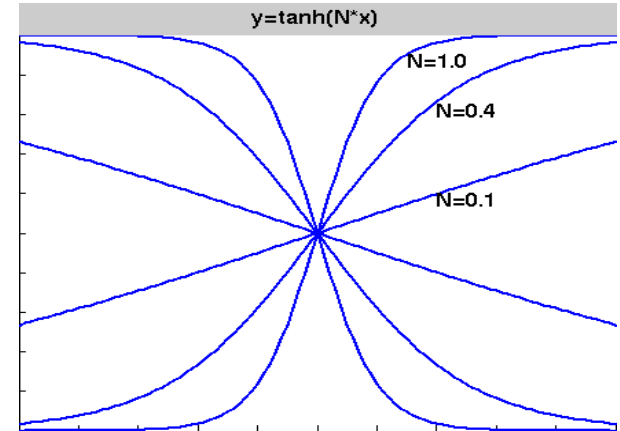
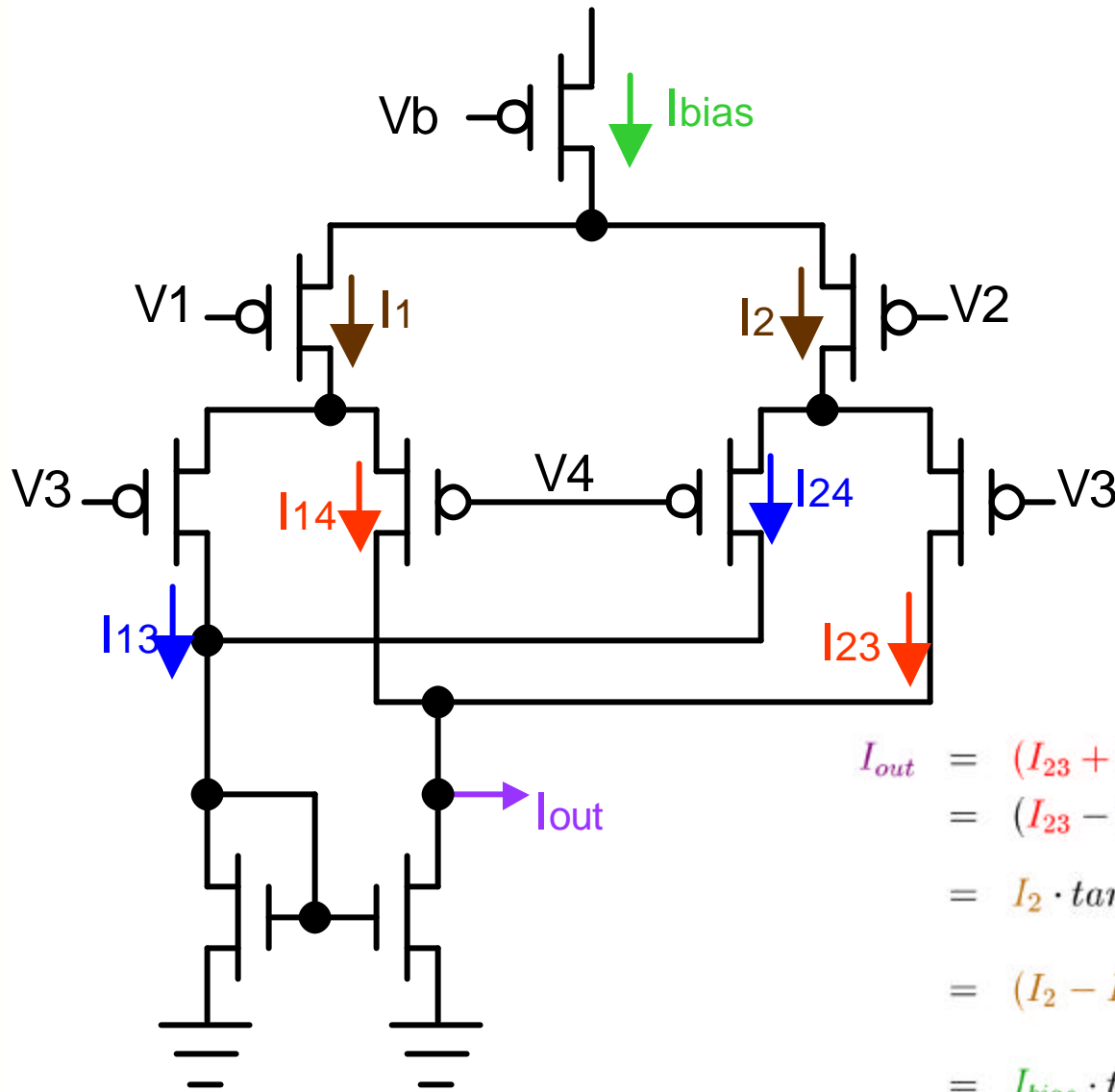
The gain is defined as:

$$\text{max output (no light)} - \text{min output (max light)}$$

The gain varies slightly as a function of the output DC voltage.



Gilbert multiplier



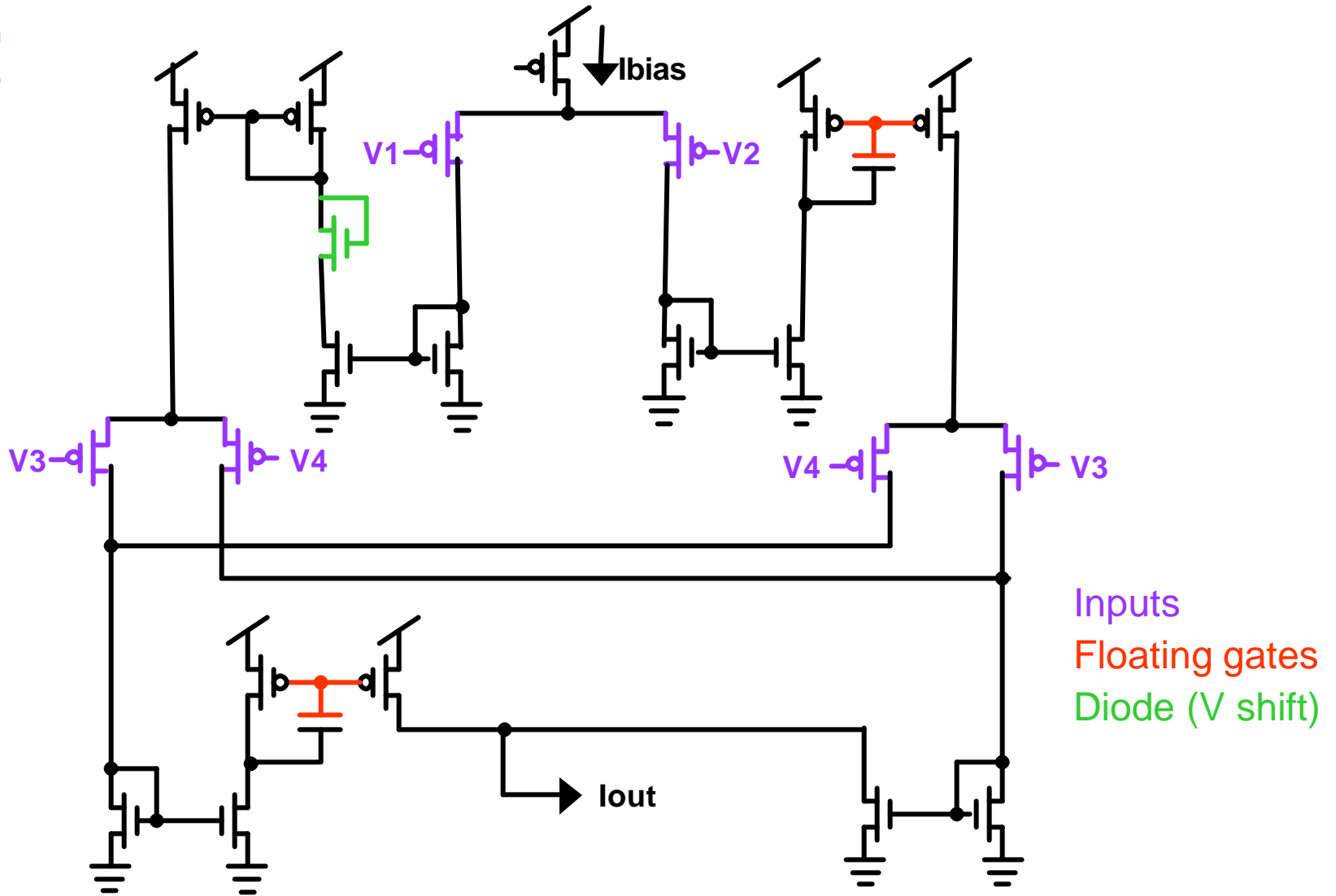
$$\begin{aligned}
 I_{out} &= (I_{23} + I_{14}) - (I_{24} + I_{13}) \\
 &= (I_{23} - I_{24}) - (-I_{14} + I_{13}) \\
 &= I_2 \cdot \tanh\left(\frac{\kappa(V_3 - V_4)}{2}\right) - I_1 \cdot \tanh\left(\frac{\kappa(V_3 - V_4)}{2}\right) \\
 &= (I_2 - I_1) \cdot \tanh\left(\frac{\kappa(V_3 - V_4)}{2}\right) \\
 &= I_{bias} \cdot \tanh\left(\frac{\kappa(V_2 - V_1)}{2}\right) \cdot \tanh\left(\frac{\kappa(V_3 - V_4)}{2}\right)
 \end{aligned}$$

Problems with Gilbert

- Limited range: Must keep all transistors in saturation; distortion
 - Limited output range: $V_{out} < V_{max} = K(\max(V3, V4) - V_b)$
 - Limited input range: similar constraint for inputs $V1$ and $V2$
- No good place to put floating gates for adaptation:
 - FG on inputs $V1$ or $V2$ results in gain mismatch between inputs
 - Since $V3$ and $V4$ go to two transistors each, we would have to have two floating gates to remove offsets between $V3$ and $V4$. Total: 3 floating gates are too many.
- Solution: use current mirrors to isolate the $V1$ - $V2$ diff pairs from $V3$ - $V4$ pairs. Increase headroom.

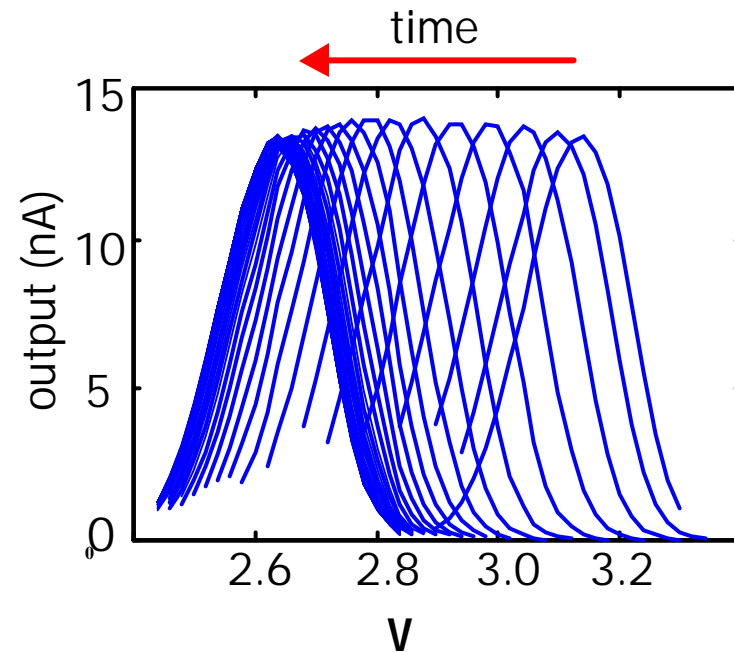
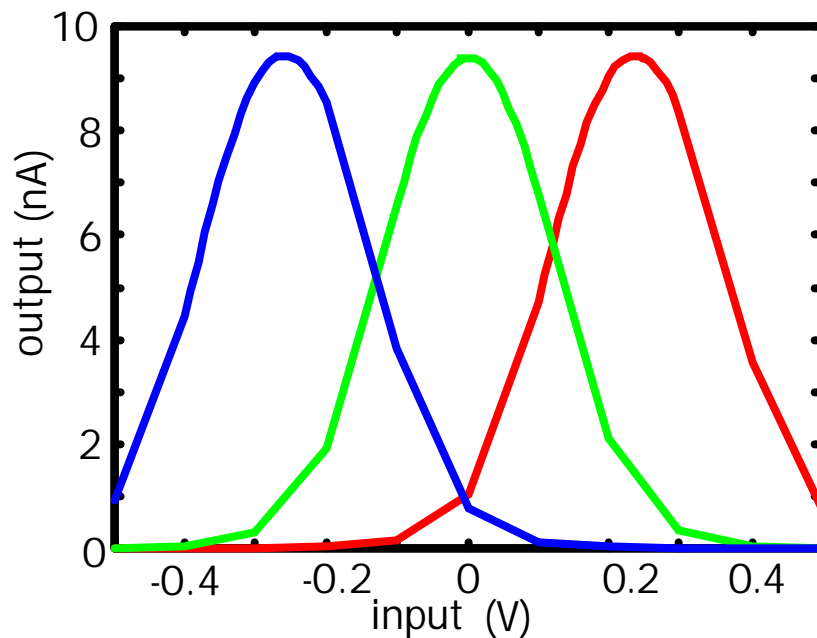


Revised multiplier

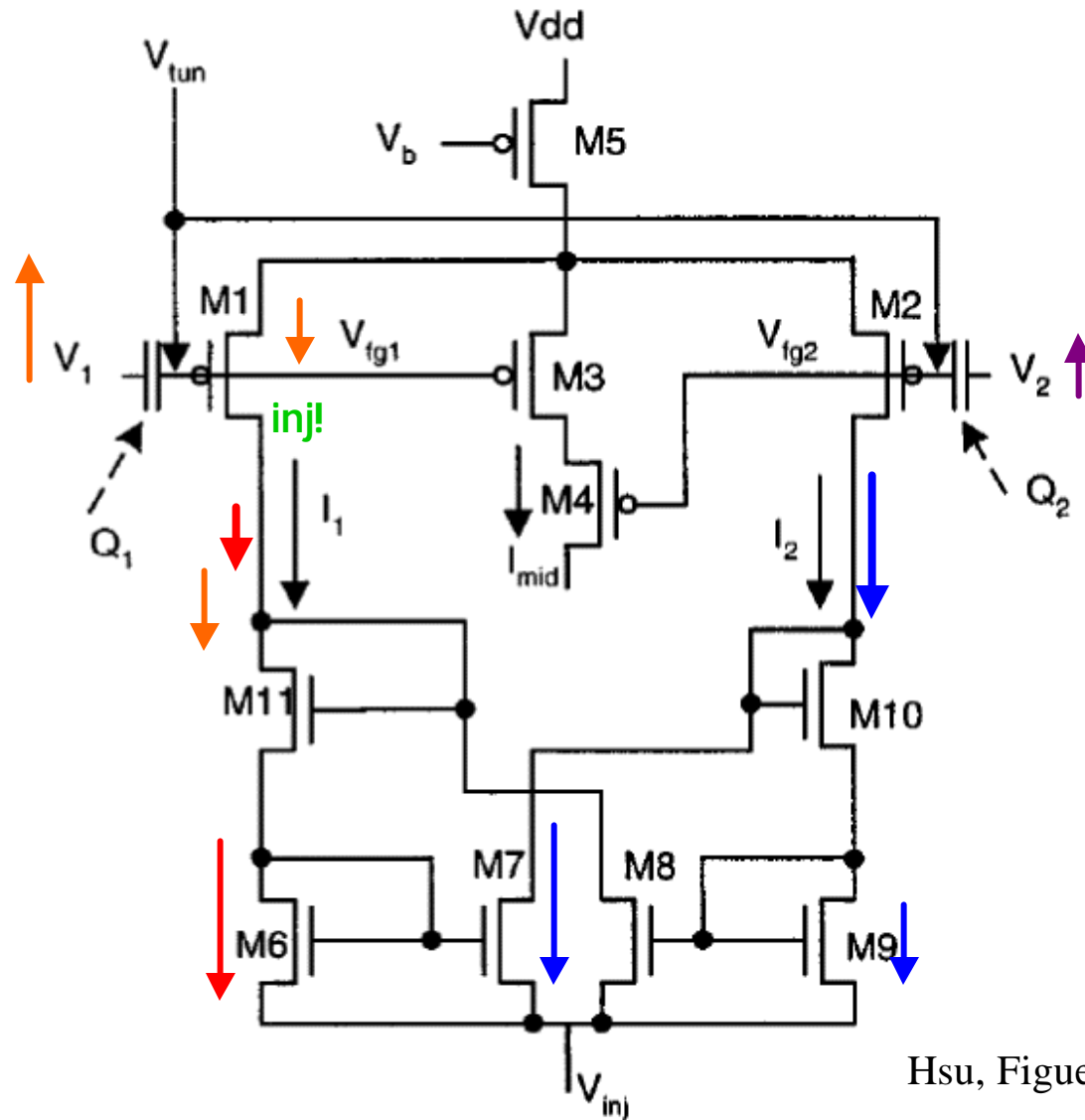


Adaptive bump circuit

- Bump circuit is a 1-D Gaussian distribution in silicon
 - Stores nonvolatile analog value μ
 - Computes Gaussian-like probability, $P(x|\mu)$
 - Adapts μ to increase $P(x|\mu)$
 - In 14 transistors

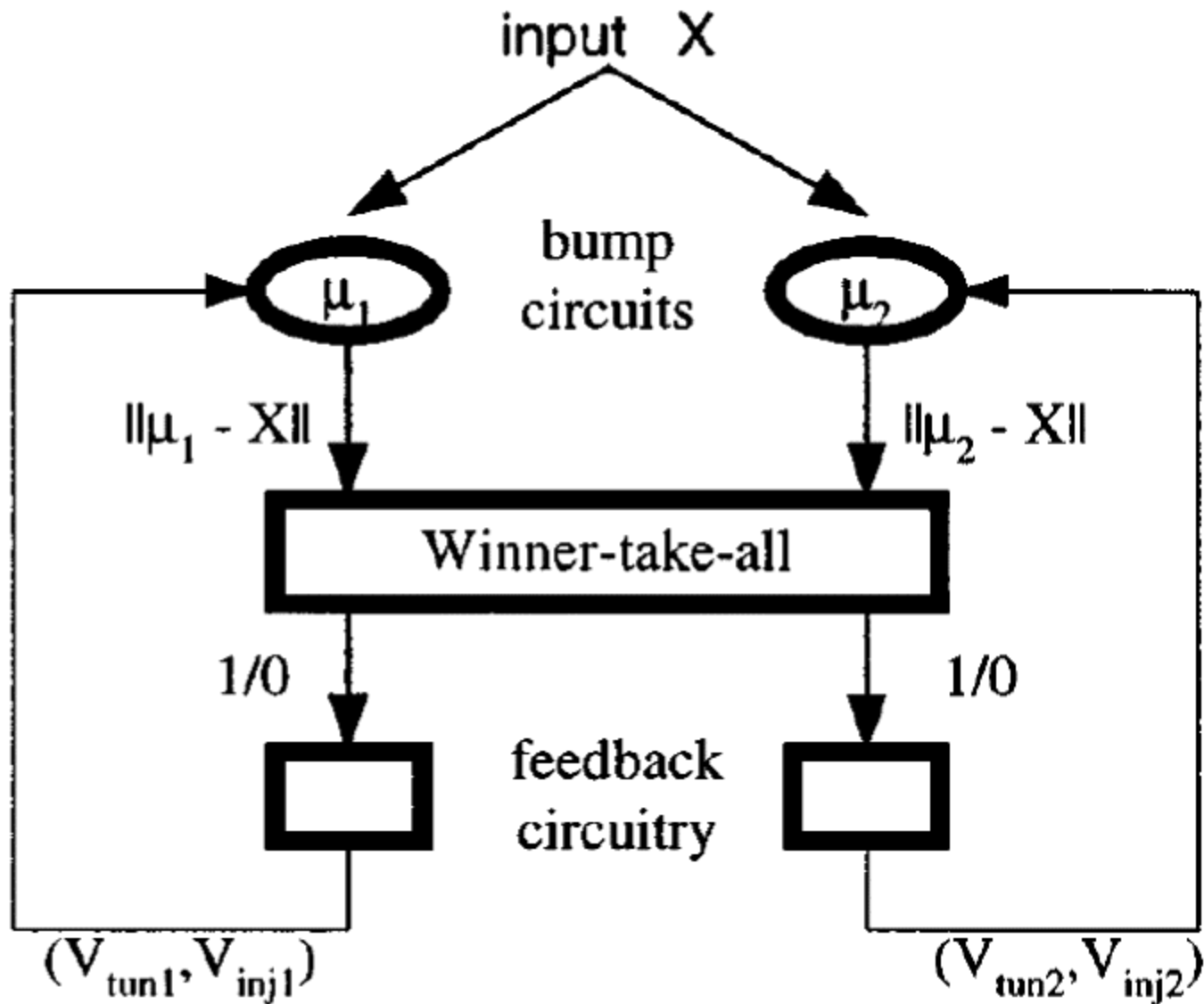


Adaptive bump circuit

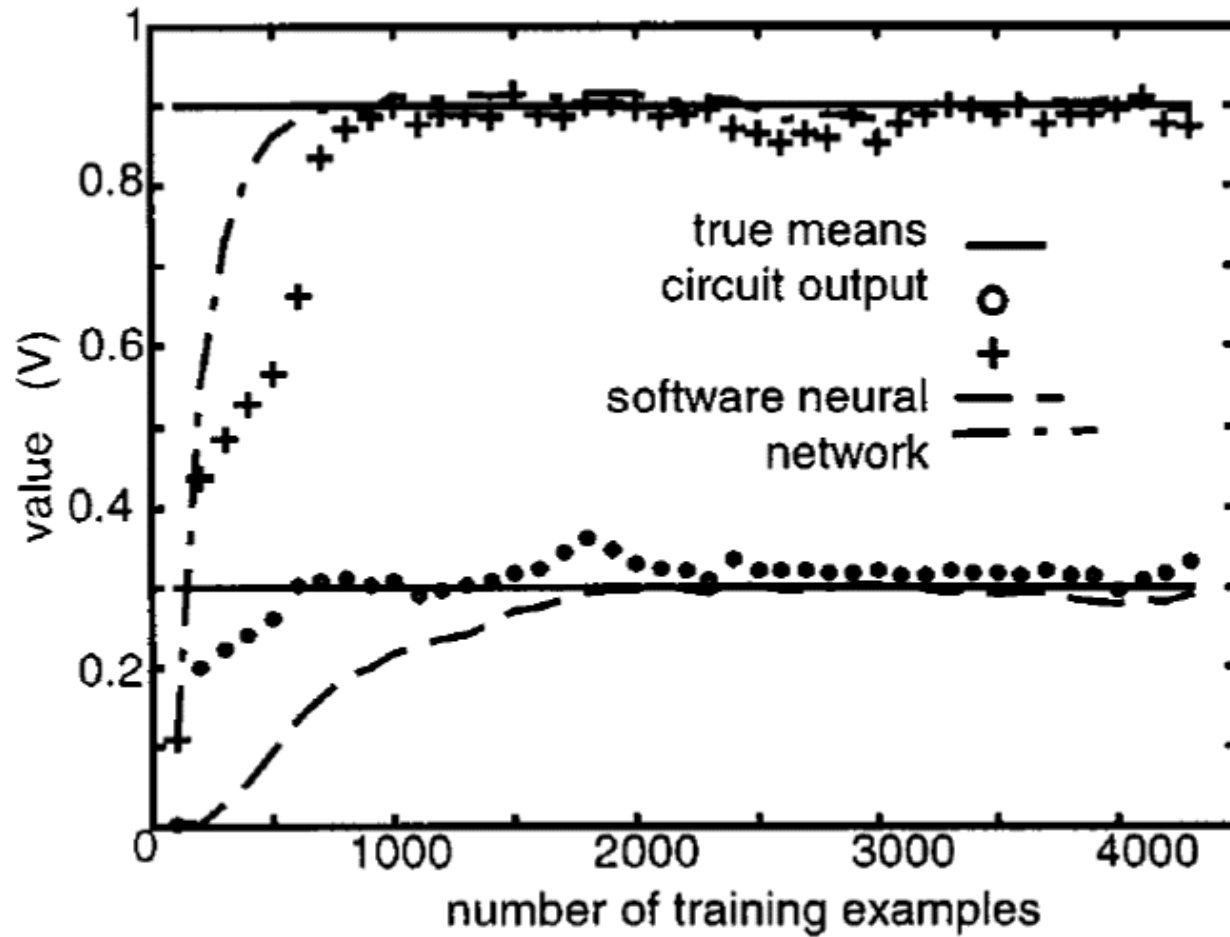


Hsu, Figueroa, Diorio 2002

Learning Mixture of Gaussians



Mixture of Gaussians data

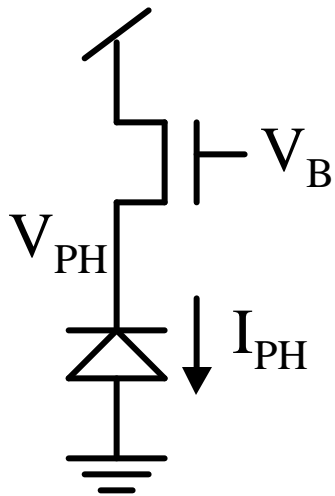


The end

Appendices follow

Photoreceptor equations

The very basic logarithmic photoreceptor:

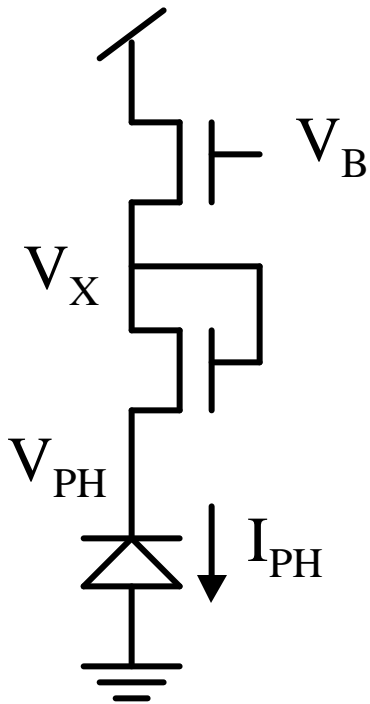


$$I_{PH} = I_0 \exp(V_B - V_{PH}) = I_0' \exp(-V_{PH})$$

$$V_{PH} = -\log\left(\frac{I_{PH}}{I_0'}\right)$$

Photoreceptor equations

Double the impedance, double the gain:



$$I_{PH} = I_0 \exp(V_B - V_X) = I_0 \exp(V_X - V_{PH})$$

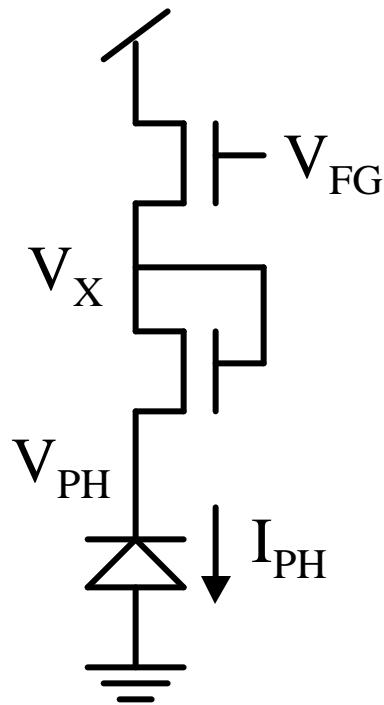
$$V_X = \frac{V_B + V_{PH}}{2}$$

$$I_{PH} = I_0 \exp\left(\frac{V_B}{2} - \frac{V_{PH}}{2}\right) = I_0' \exp\left(-\frac{V_{PH}}{2}\right)$$

$$V_{PH} = -2 \log\left(\frac{I_{PH}}{I_0'}\right)$$

Photoreceptor equations

Use a floating gate instead of a bias:



$$I_{PH} = I_0 \exp(V_{FG} - V_X) = I_0 \exp(V_X - V_{PH})$$

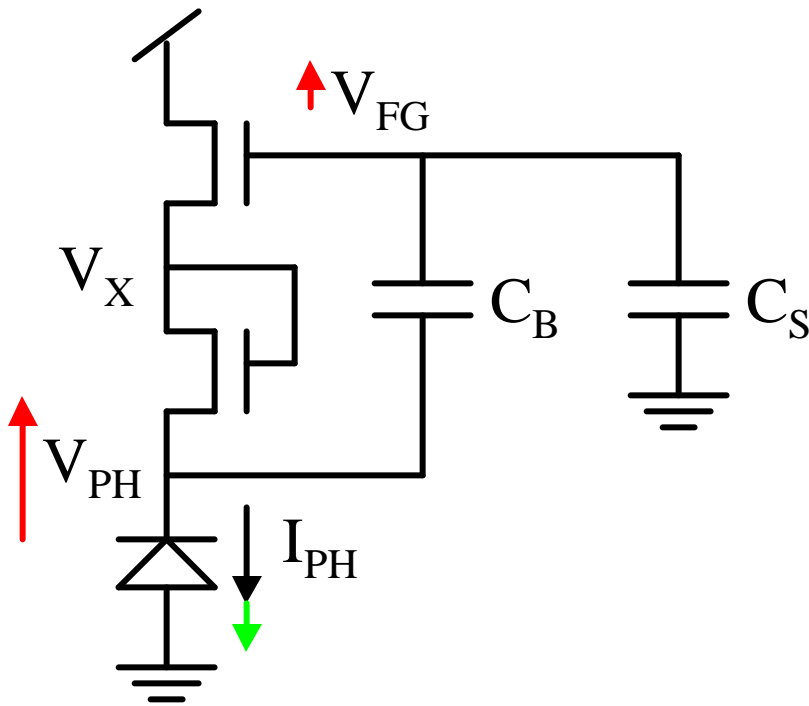
$$V_X = \frac{V_{FG} + V_{PH}}{2}$$

$$I_{PH} = I_0 \exp\left(\frac{V_{FG}}{2} - \frac{V_{PH}}{2}\right)$$

$$V_{PH} = -2 \log\left(\frac{I_{PH}}{I_0}\right) + V_{FG}$$

Photoreceptor equations

Add AC gain:



$$V_{FG} = \frac{C_B}{C_S + C_B} V_{PH}$$

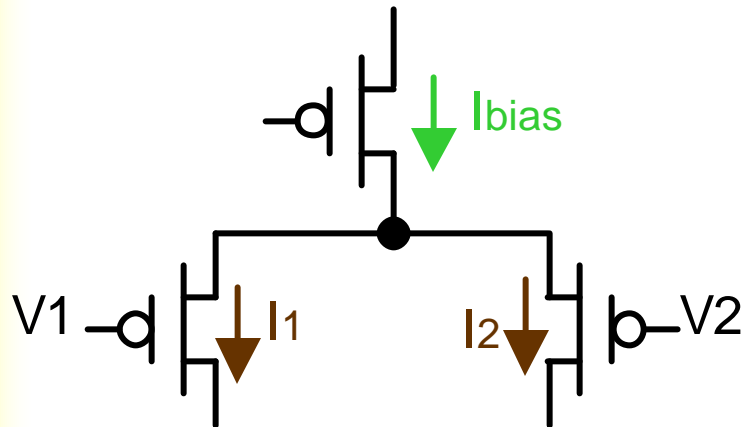
$$V_{PH} = -2 \log \left(\frac{I_{PH}}{I_0} \right) + V_{FG}$$

$$V_{PH} = -2 \log \left(\frac{I_{PH}}{I_0} \right) + \frac{C_B}{C_S + C_B} V_{PH}$$

$$V_{PH} = \frac{-2 \log \left(\frac{I_{PH}}{I_0} \right)}{1 - \frac{C_B}{C_S + C_B}}$$

$$V_{PH} = -2 \left(\frac{C_S + C_B}{C_S} \right) \log \left(\frac{I_{PH}}{I_0} \right)$$

Differential Pair



voltage-current relation in subthreshold:

$$\begin{aligned}
 I_1 &= I_o e^{(V_s - \kappa V_1)} \\
 I_2 &= I_o e^{(V_s - \kappa V_2)} \\
 I_{bias} &= I_1 + I_2 \\
 &= I_o e^{-V_s} (e^{\kappa V_1} + e^{\kappa V_2})
 \end{aligned}$$

current split between I_1 and I_2 :

$$\begin{aligned}
 I_1 &= I_{bias} \frac{e^{\kappa V_1}}{e^{\kappa V_1} + e^{\kappa V_2}} \\
 I_2 &= I_{bias} \frac{e^{\kappa V_2}}{e^{\kappa V_1} + e^{\kappa V_2}} \\
 I_1 - I_2 &= I_{bias} \frac{e^{\kappa V_1} - e^{\kappa V_2}}{e^{\kappa V_1} + e^{\kappa V_2}}
 \end{aligned}$$

multiply by $e^{-(V_1+V_2)/2}$

$$I_1 - I_2 = I_{bias} \frac{e^{\kappa(V_1-V_2)/2} - e^{\kappa(V_2-V_1)/2}}{e^{\kappa(V_1-V_2)/2} + e^{\kappa(V_2-V_1)/2}} = I_{bias} \tanh \frac{\kappa(V_1 - V_2)}{2}$$

