

Ania K. Mitros, Ph.D.

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PROFESSIONAL INTERESTS Experience designing analog VLSI circuits from a conceptual level through design and testing of fabricated chips. Recent experience in designing battery power management ICs at Maxim and testing resulting silicon. Graduate school experience in subthreshold analog design, programming floating-gate (EEPROM) devices to analog values for mismatch reduction, and analog computation in silicon; including design, layout, and testing of several chips. Look forward to working with a team of engineers to solve interesting technical challenges in analog design.

WORK AND RESEARCH EXPERIENCE

- ◇ **Analog Power Management IC Design:** (Maxim, Sept 2006–today) Work in battery power management group. Designed and tested bandgap with 1.7V supply voltage. Redesigned charge pumps for EEPROM. Co-developed an ESD diode in a high voltage process. Co-designed and tested capacitively-coupled I²C interface for MAX17068/MAX11068. Modified and tested short-circuit detection comparator. Designed and tested linear regulator. Debugged latchup and snap-back issues.
- ◇ **Feature Detector:** (Caltech/Univ. of Washington) Single-handedly designed and tested a CMOS imager chip with in-pixel analog preprocessing and floating gates (EEPROM) programmed to analog values to remove mismatch. Circuits included CMOS pixels, current-based bias generators, a sample-and-hold (S/H), sub-threshold analog circuits. Applied analog floating-gate (EEPROM) transistors to reduce mismatch in photoreceptor, Gilbert multiplier, and analog differencing circuit. This involved: Matlab system simulation, Cadence transistor-level circuit simulation and layout, microcontroller and Matlab programming for testing.
- ◇ **Vibrating Retina:** (Caltech) In a two-person team, developed on-chip imager for feature detection at sub-pixel resolution by taking advantage of mechanical vibrations. Design, transistor layout in Cadence, and testing of an asynchronous digital VLSI block for communication; testing of entire fabricated chip; AutoCAD design of mechanical system to induce the vibrations; and system simulations in Matlab. Circuits included CMOS pixels and asynchronous digital circuits.
- ◇ **Neurochip:** (Caltech, winter term 1999) Implanted neurons onto silicon chip for extracellular stimulation and recording in lab of Prof. Jerome Pine.
- ◇ **VLSI CPG:** (Los Alamos National Laboratory, summer 1997) Implemented central pattern generator (CPG) chip using discrete analog components. Learned MAGIC to design and lay out a successful CPG chip.
- ◇ **C++ Programming** (Texas Instruments, summer 1996) Wrote COFEY (Correlation Of Final Eval and Yield), an object-oriented application to extract data from two servers, perform statistical analyses, graph the data, and save it in a standard format. COFEY was in use for years.

- EDUCATION
- ◇ **California Institute of Technology. Ph.D.** in Computation and Neural Systems; advised by Professors Christof Koch (Caltech) and Chris Diorio (Univ. of Washington). Defended Feb. 15, 2006.
 - ◇ **Rice University. B.A.** Computer Science, 1998. GPA: 3.4/4.0
- PUBLISHED
- ◇ Landolt O., Mitros A. "Visual sensor with resolution enhancement by mechanical vibrations" *Autonomous Robots* (Nov 2001), 11 (3): 233-239.
 - ◇ Landolt O., Mitros A., Koch C. "Visual Sensor with Resolution Enhancement by Mechanical Vibrations" *Proceedings 2001 Conference on Advanced Research in VLSI*, 249-264.
- TEACHING
- ◇ **Workshop Tutorial** (July 2003) Taught floating gate transistor (EEPROM in analog) tutorial at the 2003 Telluride Neuromorphic Engineering Workshop, consisting of four one-hour lectures. Gave invited talk on applications of floating gates.
 - ◇ **Community Outreach** (March 2005-Aug 2006) Designed and taught hands-on lesson on electronics to kids.
 - ◇ **Teaching Assistant**
 - CNS 185 (1999): Collective Computation (neural models and neural networks)
 - CNS 187 (2000): Neural Computation (successor to CNS 185)
- SKILLS
- ◇ **Circuit design and simulation:** Cadence (primarily), Tanner Tools L-Edit, MAGIC, HSPICE
 - ◇ **Languages:** Matlab, OCEAN, C, C++, HTML, some Python
 - ◇ **Testing:** Oscilloscopes, power supplies, logic analyzer, soldering, wire wrap, etc.
 - ◇ **Failure Analysis:** emission, laser scan, liquid crystal, probing, FIB submission
- ONLINE
- ◇ http://ofb.net/~ania/ania_resume.pdf