Ania K. Mitros, Ph.D.

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Overview

Enthusiastic electrical engineer with experience in analog IC design. In addition to standard analog design skills I have experience with latchup in a high voltage process, package stress, and EEPROM devices used both for standard digital storage and analog mismatch reduction. I enjoy working with people and technical writing. I'm also inclined to think about system-level issues and the context of my project, and thus enjoy somewhat open-ended tasks where the details of the specification are partly my responsibility.

Work and Research experience

- **Maxim, Analog Power Management IC Design:** (Sept 2006–July 2013) Developed battery power management ICs, both consumer (2-4 cell) and automotive (up to 12 cell, ex. MAX11068). Standard analog design included: sub-1.7V bandgap, linear regulator, comparator, charge pumps, etc. All design work entailed supervision of layout and testing of silicon. More unique tasks included design and layout of experimental ESD structures; debugging of latchup and snap-back issues; defining an automated latchup error deck within the standard DRC flow; package stress experiments to improve stress-limited bandgap accuracy; capacitively-coupled I2C interface for the MAX11068; adapting an EEPROM block from another design group including substantial modifications while the original block was undergoing qualification and thus continual changes.
  I also contributed outside my job description. I started and lead a lunch seminar series which grew to host around 100 people. Founding member of Maxim's Green Team. Continually initiated changes by the EDA group to our internal design tools. Attended meetings of the Office of the CTO, though admit minimal impact.
- **Caltech PhD:** I designed and tested four VLSI chips with analog in-pixel image processing. Two chips were at Caltech under Prof Christof Koch, and two at the Univ. of Washington co-advised by Profs Chris Diorio and Christof Koch.
  Vibrating Retina: I developed an on-chip imager for feature detection at sub-pixel resolution by taking advantage of mechanical vibrations. Tasks included design, transistor layout in Cadence, and testing of an asynchronous digital VLSI block for communication; testing of chip; AutoCAD design of mechanical system to induce the vibrations; and system simulations in Matlab.
  Feature Detector: I designed and tested a CMOS imager chip with in-pixel analog preprocessing and floating gates (EEPROM) programmed to analog values to remove mismatch. Floating-gates reduced mismatch in photoreceptor, Gilbert multiplier, and analog differencing circuit. I used Matlab for system simulation, Cadence for transistor-level circuit simulation and layout, and microcontroller and Matlab for testing.
- **Neurochip:** (Caltech, winter term 1999) Implanted neurons onto silicon chip for extracellular stimulation and recording in lab of Prof. Jerome Pine.
- **VLSI CPG:** (Los Alamos National Laboratory, summer 1997) Implemented central pattern generator (CPG) using discrete analog components. Learned MAGIC to design and lay out a successful CPG chip.

◇ **C++ Programming** (Texas Instruments, summer 1996) Wrote COFEY (Correlation Of Final Eval and Yield), an object-oriented application to extract data from two servers, perform statistical analyses, graph the data, and save in a standard format. COFEY was in use for years.

EDUCATION

◇ **Online, Sept-Dec 2013**

- "Introduction to Power Electronics" by Prof Erickson at UC Boulder via Coursera
- "Solar Cells, Fuel Cells and Batteries" by Prof Clemens at Stanford via Stanford OpenEdX
- "Inspiring Leadership through Emotional Intelligence" by Prof Boyatzis at Case Western via Coursera

◇ **California Institute of Technology Ph.D.** in Computation and Neural Systems; advised by Professors Christof Koch (Caltech) and Chris Diorio (Univ. of Washington). Defended Feb. 15, 2006.

◇ **Rice University B.A.** Computer Science, 1998. GPA: 3.4/4.0

PUBLISHED

◇ **L**andolt O., Mitros A. "Visual sensor with resolution enhancement by mechanical vibrations" *Autonomous Robots* (Nov 2001), 11 (3): 233-239.

◇ **L**andolt O., Mitros A., Koch C. "Visual Sensor with Resolution Enhancement by Mechanical Vibrations" *Proceedings 2001 Conference on Advanced Research in VLSI*, 249-264.

TEACHING

◇ **Workshop Tutorial** (July 2003) Taught floating gate transistor (EEPROM in analog) tutorial at the 2003 Telluride Neuromorphic Engineering Workshop, consisting of four one-hour lectures. Gave invited talk on applications of floating gates.

◇ **Community Outreach** (March 2005-Aug 2006) Designed and taught hands-on lesson on electronics to kids.

◇ **Teaching Assistant**

- CNS 185 (1999): Collective Computation (neural models and neural networks)
- CNS 187 (2000): Neural Computation (successor to CNS 185)

SKILLS

◇ **P**roficient: Cadence schematic, simulation, layout; Matlab; HTML

◇ **A**dequate: OCEAN; C; C++; Python; Altium for PCB layout

◇ **F**ailure Analysis: emission, laser scan, liquid crystal, probing, FIB submission

ONLINE

◇ **T**his resume online: http://ofb.net/~ania/AniaMitros_resume.pdf