# Ania K. Mitros, Ph.D.

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## Overview

Electrical engineer experienced with battery management systems (BMS), including high voltage automotive and 50V home energy storage batteries. I have seen the full BMS and BMS chip development cycles: definition, design, and production. I have defined and analyzed BMS safety architecture under ISO-26262 and per internal goals.

My favorite job was at Tesla, where I was responsible for the ASICs at the core of a more accurate, more robust, and less costly BMS than the previous generation. I enjoyed the mix of breadth and depth: system-level challenges mixed with deep dives into data and design. The role was a lovely balance of collaboration across teams and individual work.

## Work and Research experience

- **Zitara** (Sep 2024–present) At this software-focused company, my hardware perspective helps assess impact of sensor error on state estimation accuracy.
- **Lunar Energy** (Mar 2021–Aug 2022) Responsible for BMS of the home energy storage system including architecture, schematic review, safety analysis, and defining fault thresholds. Tested the BMS hardware. Mentored junior engineers.
- **Tiveni** (Feb 2020–Jun 2020) Second member of the two-person all-woman EE team! Involved in BMS architecture, system analysis, and PCB schematics.
- **Continental Automotive** (May 2018–Jan 2020) Though hired into the innovation organization, I worked closely with product design groups. I was the main liaison to an ASSP partner, performed system and safety analyses, precision measurements, assessed alterative ASSPs, and evaluted safety under ISO-26262.
- **Tesla Battery Engineering:** (Oct 2014–Apr 2018) I led Tesla's first custom ASIC project: the ASICs that measure voltages and temperatures in the Model 3 high voltage battery. My role included the full product cycle: requirement definition, cost trade-offs, vendor selection, PCBA design review, fault tree analysis, diagnostics definition, collaboration with firmware, legal contract development, Python and MySql to analyze vehicle field data and manufacturing test data, analysis of test data, setting manufacturing test limits, reliability evaluation, introduction to mass production, and general shepherding.
- **Maxim, Analog Power Management IC Design:** (Sept 2006–July 2013) I designed analog circuits inside BMS chips, both consumer (2-4 cell) and automotive (12 cell: MAX11068, MAX17823), and did some R&D projects. My circuits included: sub-1.7V bandgap, linear regulator, comparator, charge pumps, redesign of an EEPROM block from another design group while the original block was in qualification and changing, capacitively-coupled I2C interface for the MAX11068, supervision of layout, bench testing of silicon. R&D tasks included design and layout of experimental ESD structures, debugging of latchup and snap-back in a high voltage process, defining an automated latchup error deck within the standard DRC flow, and package stress experiments to improve reference accuracy.

  Additionally, I started and led a lunch seminar series which grew to around 100 participants. Founding member of Maxim's Green Team. Continually initiated changes by the EDA group to our internal design tools.

- **Caltech PhD:** I designed and tested four VLSI chips with analog in-pixel image processing under Profs Christof Koch at Caltech and Chris Diorio at the Univ. of Washington. *Vibrating Retina:* A chip for feature detection with sub-pixel resolution exploiting mechanical vibrations, incorporating asynchronous digital communications.
  *Feature Detector*: CMOS imager chip with in-pixel analog preprocessing and floating gates (EEPROM) programmed to analog values to remove mismatch. Floating-gates reduced mismatch in photoreceptor, Gilbert multiplier, and analog differencing circuit.
- **Neurochip:** (Caltech, winter term 1999) Implanted neurons onto silicon chip for extracellular stimulation and recording in lab of Prof. Jerome Pine.
- **VLSI CPG:** (Los Alamos National Laboratory, summer 1997) Implemented central pattern generator (CPG) using discrete analog components. Learned MAGIC to design and lay out a successful CPG chip.
- **C++ Programming** (Texas Instruments, summer 1996) Wrote COFEY (Correlation Of Final Eval and Yield), an object-oriented application to analyze, graph, and export data from two servers. COFEY was in use for years.

## Education

- **California Institute of Technology Ph.D.** in Computation and Neural Systems. 2006.
- **Rice University B.A.** Computer Science, 1998.
- **Westlake High School.** 1994. Class rank: 9/406
- **Online** Sept-Dec 2013
  - "Introduction to Power Electronics" by Prof Erickson, UC Boulder, Coursera
  - "Solar Cells, Fuel Cells and Batteries" by Prof Clemens, Stanford OpenEdX
  - "Inspiring Leadership through Emotional Intelligence" by Prof Boyatzis, Case Western, Coursera

## Published

- **B**ement *et al.* "Filtration and Breathability of Nonwoven Fabrics Used in Washable Masks" *Aerosol and Air Quality Research* (Sep 2022), 22 (9). doi.org/10.4209/aaqr.220044
- **L**andolt O., Mitros A. "Visual sensor with resolution enhancement by mechanical vibrations" *Autonomous Robots* (Nov 2001), 11 (3): 233-239.
- **L**andolt O., Mitros A., Koch C. "Visual Sensor with Resolution Enhancement by Mechanical Vibrations" *Proceedings 2001 Conference on Advanced Research in VLSI*, 249-264.

## Teaching

- **Ania's BMS Course** (ongoing) Online videos to train the next generation of BMS engineers. http://ofb.net/~ania/Anias-BMS-Course
- **Workshop Tutorial** (July 2003) Taught floating gate transistor tutorial at 2003 Telluride Neuromorphic Engineering Workshop.
- **Community Outreach** (March 2005-Aug 2006) Designed and taught hands-on lesson on electronics to kids.
- **Teaching Assistant**
  - CNS 185 (1999): Collective Computation (neural models and neural networks)
  - CNS 187 (2000): Neural Computation (successor to CNS 185)